What is claimed is:

1. A combination, comprising:

a processor; and

a transparent memory array comprising a plurality of memory banks, each of said plurality of memory banks being directly connected to said processor, said memory array operable to function without at least one of a precharge signal, a row address latch signal, and a column address latch signal.

2. The combination of claim 1 wherein said processor is operable to simultaneously communicate with at least two of said plurality of memory banks.

3. The combination of claim 1 wherein one of said plurality of memory banks further comprises at least one of a row address decoder, a column address decoder, and a controller.

4. The combination of claim 1 wherein said processor provides at least one of a row address signal and a column address signal to said plurality of memory banks, said row address signal having a row address latency period being dependent primarily on a row address decoding pipeline and said column address signal having a column address latency period being dependent primarily on a column address decoding pipeline.

5. The combination of claim 1 wherein one of said plurality of memory banks is a synchronous dynamic random access memory.

6. A combination, comprising:

a processor; and

a plurality of transparent memory arrays being directly connected to said processor, and each operable to function without at least one of a precharge signal, a row address latch signal, and a column address latch signal.

7. The combination of claim 6 wherein said processor is operable to simultaneously communicate with at least two of said plurality of transparent memory arrays.

8. The combination of claim 6 wherein one of said plurality of transparent memory arrays further comprises at least one of a row address decoder, a column address decoder, a controller, and a plurality of individual memory cells.

9. The combination of claim 6 wherein said processor provides at least one of a row address signal and a column address signal to said plurality of memory banks, said row address signal having a row address latency period being dependent primarily on a row address decoding pipeline and said column address signal having a column address latency period being dependent primarily on a column address decoding pipeline.

10. The combination of claim 1 wherein one of said plurality of transparent memory arrays is a synchronous dynamic random access memory.

11. A combination comprising:

an integrated circuit having a processor; and

an embedded memory array, said memory array having a plurality of controllers and a plurality of memory banks, each of said memory banks being independently connected to one of said plurality of controllers, each of said controllers being independently connected to said processor.

12. The combination of claim 11 wherein the memory array further comprises:

a plurality of row address decoders, each of said row address decoders being connected to one of said memory banks and to one of said controllers; and

a plurality of column address decoders, each of said column address decoders being connected to one of said memory banks and to one of said controllers.

13. The combination of claim 11 wherein the memory array further comprises:

a data bus having a plurality of data lines, at least one of said plurality of data lines being connected to each of said memory banks.

14. The combination of claim 13 wherein said data bus is operable to simultaneously receive data from each of said memory banks.

15. The combination of claim 13 wherein said data bus is operable to simultaneously provide data to each of said memory banks.

16. The combination of claim 12 wherein said processor is operable to simultaneously send address information to more than one of said plurality of row address decoders and said plurality of column address decoders.

17. The combination of claim 11 wherein said embedded memory array is comprised of synchronous dynamic random access memory.

18. A combination comprising:

an integrated circuit having a processor; and

an embedded memory array, said memory array having a plurality of memory banks, each of said memory banks being independently connected to said processor.

19. The combination of claim 18 wherein the memory array further comprises:

a plurality of controllers, each of said plurality of controllers being independently connected to said processor;

a plurality of row address decoders, each of said row address decoders being connected to one of said memory banks and to one of said controllers; and

a plurality of column address decoders, each of said column address decoders being connected to one of said memory banks and to one of said controllers.

20. The combination of claim 18 wherein the memory array further comprises:

a data bus having a plurality of data lines, at least one of said plurality of data lines being connected to each of said memory banks.

21. The combination of claim 20 wherein said data bus is operable to simultaneously receive data from each of said memory banks.

22. The combination of claim 20 wherein said data bus is operable to simultaneously provide data to each of said memory banks.

23. The combination of claim 19 wherein said processor is operable to simultaneously send address information to more than one of said plurality of controllers.

24. The combination of claim 18 wherein said embedded memory array is comprised of synchronous dynamic random access memory.

25. A combination, comprising:

a processor; and

a plurality of transparent SDRAM arrays directly connected to said processor.

26. The combination of claim 25 wherein each of said plurality of transparent SDRAM memory arrays further comprises:

a plurality of memory banks;

a plurality of controllers, each of said plurality of controllers being independently connected to said processor and to one of said plurality of memory banks;

a plurality of row address decoders, each of said row address decoders being connected to one of said plurality of memory banks and to one of said controllers; and

a plurality of column address decoders, each of said column address decoders being connected to one of said plurality of memory banks and to one of said controllers.

27. The combination of claim 26 wherein the transparent SDRAM memory array further comprises:

a data bus having a plurality of data lines, at least one of said plurality of data lines being connected to each of said plurality of memory banks.

28. The combination of claim 27 wherein said data bus is operable to simultaneously receive data from each of said plurality of memory banks.

29. The combination of claim 27 said data bus is operable to simultaneously provide data to each of said plurality of memory banks.

30. The combination of claim 26 wherein said processor is operable to simultaneously send address information to more than one of said plurality of controllers.

31. A combination, comprising:

a processor; and

a transparent SDRAM having a plurality of memory banks, each of said plurality of memory banks being directly connected to said processor.

32. The combination of claim 31 wherein each of said plurality of transparent SRAM memory arrays further comprises:

a plurality of controllers, each of said plurality of controllers being independently connected to said processor and to one of said plurality of memory banks;

a plurality of row address decoders, each of said row address decoders being connected to one of said plurality of memory banks and to one of said controllers; and

a plurality of column address decoders, each of said column address decoders being connected to one of said plurality of memory banks and to one of said controllers.

33. The combination of claim 32 wherein the memory array further comprises:

a data bus having a plurality of data lines, at least one of said plurality of data lines being connected to each of said plurality of memory banks.

34. The combination of claim 33 wherein said data bus is operable to simultaneously receive data from each of said plurality of memory banks.

35. The combination of claim 33 wherein said data bus is operable to simultaneously provide data to each of said plurality of memory banks.

36. The combination of claim 32 wherein said processor is operable to simultaneously send address information to more than one of said plurality of controllers.

37. A combination, comprising:

a processor; and

a transparent SDRAM having a plurality of memory banks connected to said processor such that said processor may simultaneously access more than one of said plurality of memory banks.

38. The combination of claim 37 wherein each of said plurality of transparent SDRAM memory arrays further comprises:

a plurality of controllers, each of said plurality of controllers being independently connected to said processor and to one of said plurality of memory banks;

a plurality of row address decoders, each of said row address decoders being connected to one of said plurality of memory banks and to one of said controllers; and

a plurality of column address decoders, each of said column address decoders being connected to one of said plurality of memory banks and to one of said controllers.

39. The combination of claim 38 wherein the transparent SDRAM memory array further comprises:

a data bus having a plurality of data lines, at least one of said plurality of data lines being connected to each of said plurality of memory banks.

40. The combination of claim 39 wherein said data bus is operable to simultaneously receive data from each of said plurality of memory banks.

41. The combination of claim 39 wherein said data bus is operable to simultaneously provide data to each of said plurality of memory banks.

42. The combination of claim 38 wherein said processor is operable to simultaneously send address information to more than one of said plurality of controllers.

43. A transparent memory array comprising:

a plurality of memory banks each comprised of a plurality of memory cells; and

a plurality of peripheral devices for writing information into and reading information out of said memory cells, said plurality of peripheral devices including a plurality of controllers, one of each said plurality of controllers connected to one of each said plurality of memory banks, and wherein said plurality of controllers is operable to simultaneously communicate with a processor.

44. The transparent memory array of claim 43 wherein said plurality of peripheral devices further comprises:

a plurality of row address decoders, each of said plurality of row address decoders having a row address input bus and a row address output bus, at least one of said plurality of row address decoders having said row address input bus connected to one of said plurality of controllers and having said row address output bus connected to one of said plurality of memory banks; and

a plurality of column address decoders, each of said plurality of column address decoders having a column address input bus and a column address output bus, at least one of said plurality of column address decoders having said column address input bus connected to said at least one of said plurality of controllers and having said column address output bus connected to said at least one of said plurality of memory banks.

45. The transparent memory array of claim 43 wherein said plurality of controllers are operable to simultaneously exchange at least one of address information and data with a processor.

46. The transparent memory array of claim 43 wherein said plurality of controllers are operable to simultaneously exchange at least one of address information and data with said plurality of memory banks.

47. The transparent memory array of claim 43 further comprising a data bus, said data bus having a plurality of data lines connected with each of said plurality of memory banks, said data bus operable to simultaneously carry data signals from each of said plurality of memory banks.

48. The transparent memory array of claim 43 wherein at least two of said memory arrays have a different data signal burst mode.

49. A method for decreasing the access latency of an integrated circuit having a processor and a plurality of embedded memory arrays, said plurality of memory arrays having a plurality of memory banks, said method comprising:

connecting each of said plurality of memory banks to said processor; and

simultaneously accessing at least two of said plurality of embedded memory banks with said processor.

50. The method of claim 49 wherein said connecting step further comprises:

connecting each of said plurality of memory banks to one of a plurality of row address decoders, said one of said plurality of row address decoders being connected to said processor; and

connecting each of said plurality of memory banks to one of a plurality of column address decoders, said one of said plurality of column address decoders being connected to said processor.

51. The method of claim 49 wherein said simultaneously accessing step further comprises at least one of:

simultaneously exchanging row address information between said processor and more than one of said plurality of row address decoders;

simultaneously exchanging column address information between said processor and more than one of said plurality of column address decoders; and

simultaneously exchanging data between said processor and more than one of said plurality of memory banks.

52. A method for increasing the throughput of an integrated circuit having a processor and an transparent SDRAM array, said transparent SDRAM array having a controller, a data bus, and a plurality of memory banks, each of said plurality of memory banks being independently connected to said controller, said method comprising at least one of:

simultaneously reading data from more than one of said plurality of memory banks; and

simultaneously writing data from more than one of said plurality of memory banks.

53. The method of claim 52 wherein said simultaneously reading step further comprises:

simultaneously exchanging read address information between said processor and more than one of said plurality of memory banks; and

providing a data signal from said more than one of said plurality of memory banks to said data bus.

54. The method of claim 52 wherein said simultaneously writing step further comprises:

simultaneously exchanging write address information between said processor and said more than one of said plurality of memory banks;

providing a data signal from said data bus to said more than one of said plurality of memory banks.

55. The method of claim 53 wherein each of said memory banks has a row address decoder and a column address decoder associated therewith, said exchanging read address information step further comprises:

transmitting a first row address information from said processor to a first row address decoder;

transmitting a first column address information from said processor to a first column address decoder; and

simultaneously transmitting at least one of another row address information and column address information from said processor to at least one of another row address decoder and another column address decoder.

56. The method of claim 54 wherein said providing a data signal from said more than one of said plurality of memory banks to said data bus further comprises:

simultaneously decoding said read address information exchanged between said processor and said more than one of said memory banks;

selecting a memory cell within each of said more than one of said memory banks based on said read address information; and

simultaneously reading said data signal from said selected memory cells within said more than one of said plurality of memory banks.

57. The method of claim 54 wherein each of said memory banks has a row address decoder and a column address decoder associated therewith, said exchanging write address information step further comprises:

transmitting a first row address information from said processor to a first row address decoder;

transmitting a first column address information from said processor to a first column address decoder; and

simultaneously transmitting at least one of another row address information and column address information from said processor to at least one of another row address decoder and another column address decoder.

58. The method of claim 54 wherein said providing a data signal from said data bus to said more than one of said plurality of memory banks further comprises:

simultaneously decoding said write address information exchanged between said processor and said more than one of said memory banks;

selecting a memory cell within said each of said more than one of said memory banks based on said write address information; and

simultaneously writing said data signal from said data bus within each of said selected memory cells.